Development and Exploitation of Processes For Thin Flexible Glass

Wednesday 14th May 2014

ATOTECH

Plating on Glass

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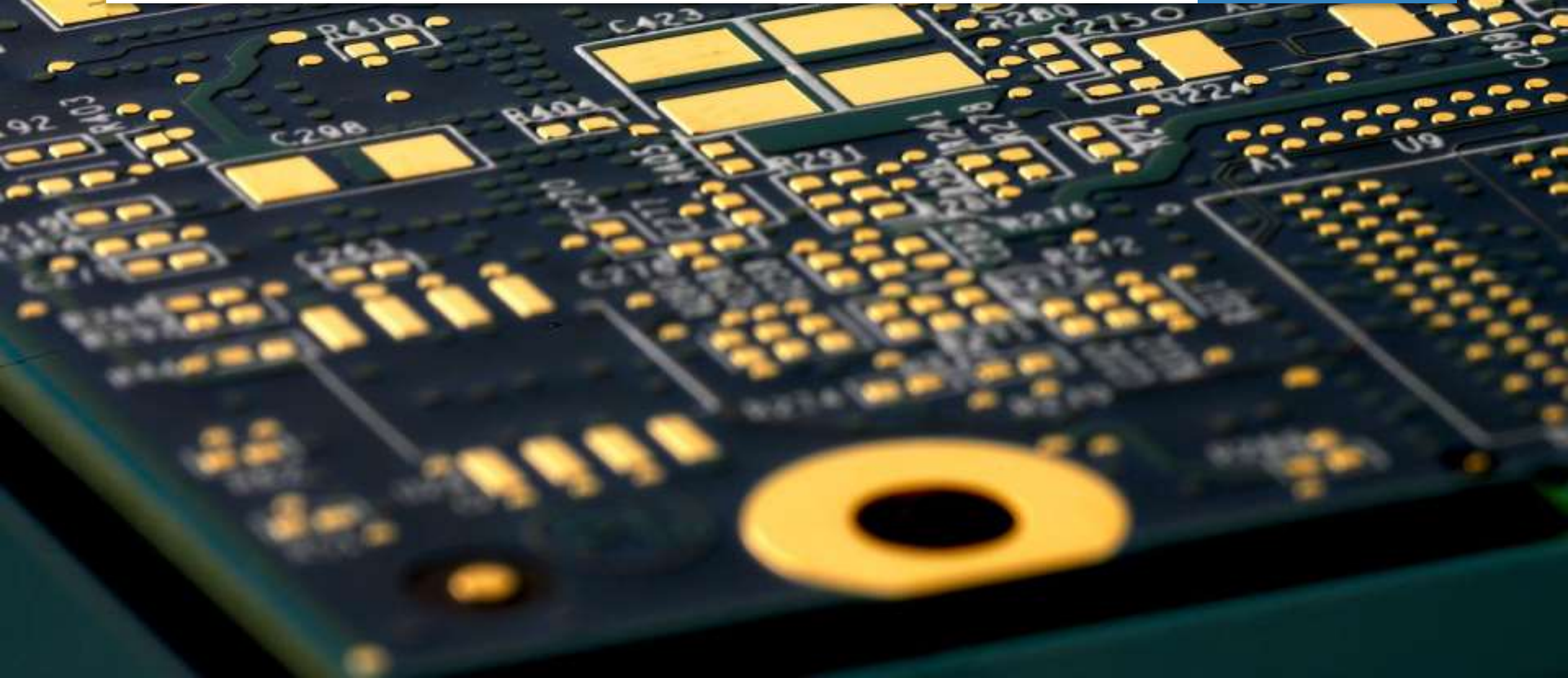
Electronics

Plating on Glass

Overview and Process Technologies

2014.05.13_PoG_Overview MSolv_ART



Plating on Glass
Scope

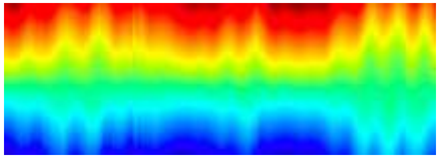
- Market Trends / Motivation

- Applications

- Manufacturing Methods

- Through Hole Filling

- Electrical Characterization



- Summary

Plating on Glass

Market Trends - Electronics Evolution

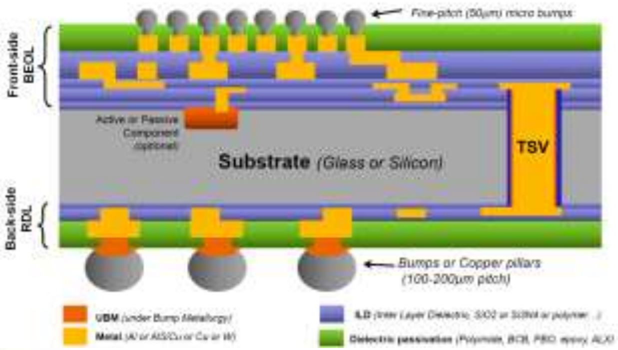
PCB

OSAT

Wafer Foundry

Organic Substrate

Si/Glass Interposer



(Source: Yole)

Gap !

PCB Design Rule

Wafer Design Rule

100µm — 10µm — 1µm — 100nm — 10nm

Foundry, OSAT and PCB Companies Need New Processes to Fill the Gap

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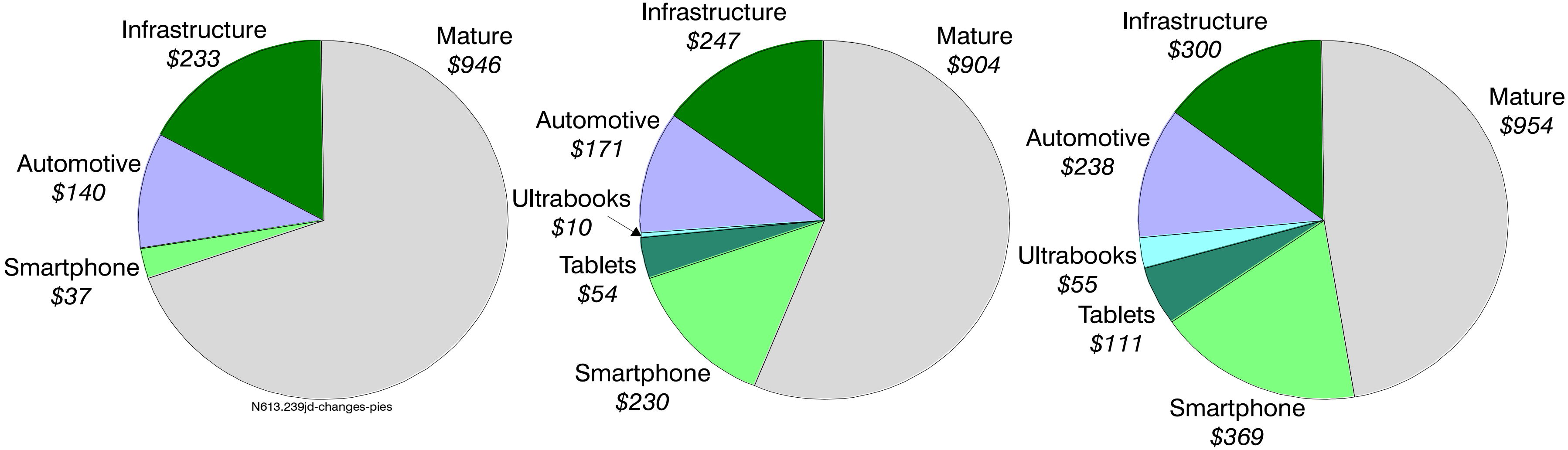
Plating on Glass
Market Trends

CHANGES IN THE ELECTRONICS INDUSTRY STRUCTURE

2007 **2012** **2017F**



Total: $1,356Bn **Total: $1,616Bn** **Total: $2,027Bn**

	CAAGR 2007-2012	CAAGR 2012-2017	CAAGR 2007-2017
Mature	-0.9%	1.1%	0.1%
Growth	11.8%	8.5%	10.1%
Total	3.6%	4.6%	4.1%

Major Growth Areas in Mobile Formats – Smartphone – Tablets

Plating on Glass
Market Trends

- Major growth is all in mobile sector
- Smartphone growth:
  – 2012 - 2013 -15.7%
  – CAGR 2012 - 2017 - **9.9%**
- Tablet growth:
  – 2012 - 2013 - 46.3%
  – CAGR 2012 - 2107 - **15.6%**
- Ultrabook growth:
  – 2012 - 2013 - 80.1%
  – CAGR 2012 - 2017 - **40.6%**
- Servers and Automotive will see steady growth
  – Cloud computing and automotive electronics
- Rest of Electronics Industry will stagnate

Apple iPhone 5S

Apple iPad Mini

Major Growth Areas in Mobile Formats – Smartphone – Tablets

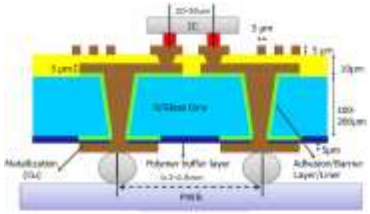
Plating on Glass
Motivation

- TFT Metallization for Flat Panel Displays
  – Sputtered seed layers (Mo, Ti/Cu)
  – Electroless Copper deposition (Up to 2 µm)
  – Electrolytic Copper plating (2 – 20 µm)

- Metallization for Touch Screens
  – Electroless Copper for improved conductivity

- Glass Metallization for Photovoltaic Applications
  – Electroless Copper on plain glass
  – Backplane electrode metallization

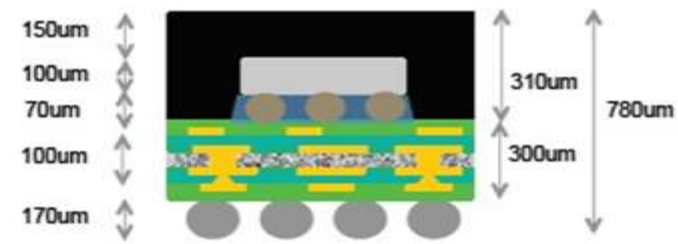
- Glass Metallization for Advanced Chip Packaging
  – Sputtered seed layers (Ti/Cu) or plain glass
  – Adhesion promoters for direct plating of electroless
  – Electroless and Electrolytic Copper for Glass interposer



Source: PRC at Georgia Tech

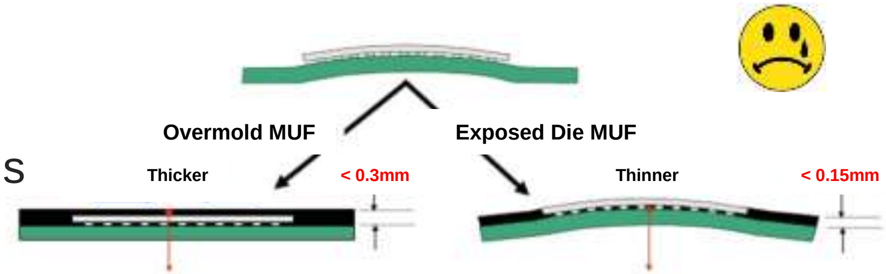
Plating on Glass
Motivation

- Mobile Device Packaging
  - Handset thickness approaching 6mm
  - Battery and screen size increasing
  - Chip packaging and the substrate board must shrink to accommodate this



Solder Balls Significant Proportion of Package Height

- Warpage Reduction
  - Core thickness, CTE and modulus key
  - Core CTE already at 3ppm
    - Further reduction is no longer an option
  - Industry needs materials of higher modulus



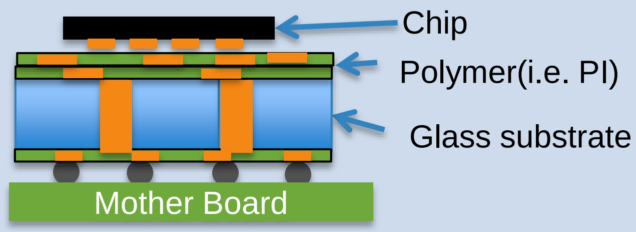
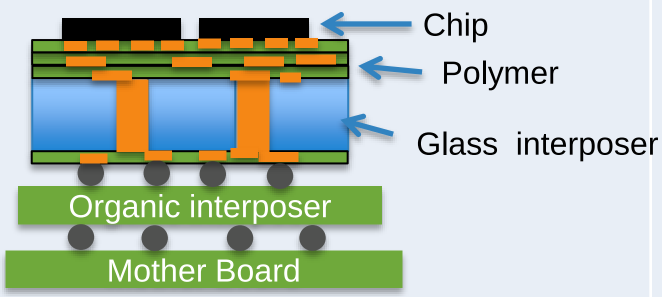
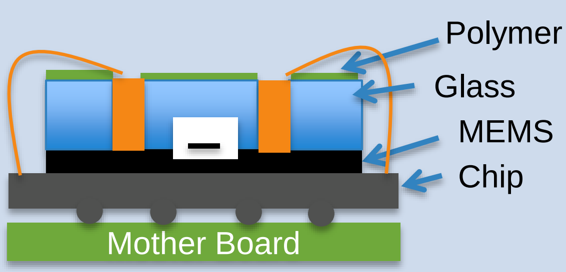
Low Cry Warpage Essential for Thinner Packages

Source: Qualcomm

- Pitch Requirement Reducing
  - Fine pitch requires copper pillar connections
  - Thermocompression bonding essential
  - Thinner Molding Compound increases warpage
  - Higher Mold shrinkage and modulus also required

MUF – Molded Underfill

Plating on Glass
Possible Applications

Category	Structure	Application
Glass substrate		RF module
Interposer		2.5/3D packaging
3D WLP		MEMS

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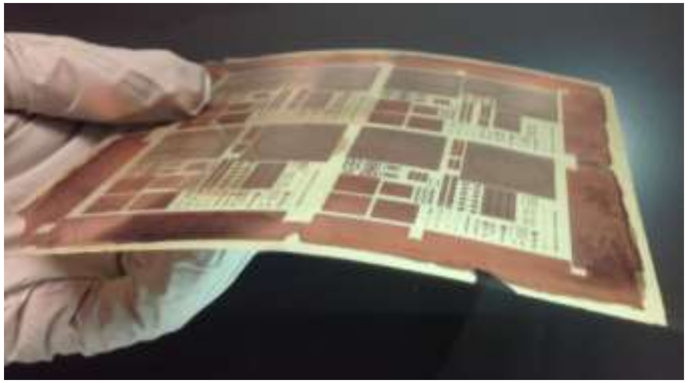
Manufacturing Methods

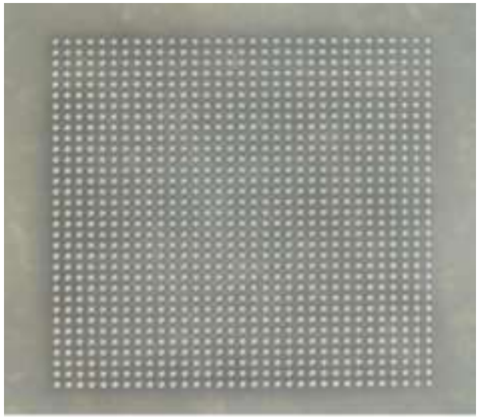
Plating on Glass
Manufacturing Methodologies

- Sputtering of seed layer directly onto glass
  - Aspect ratio issues
  - Variable adhesion
- Nano Particle Inks
- Polymer Laminated Glass
  - Georgia Tech Consortia
- VitroCoat Adhesion Promoter
  - Metal Oxide based adhesion promoter
  - Suitable for glass and ceramics

(Source: Georgia Tech)



30µm Thick Polymer Laminated Glass



1089 Via Drilled Simultaneously

(Source: Asahi Glass Company)

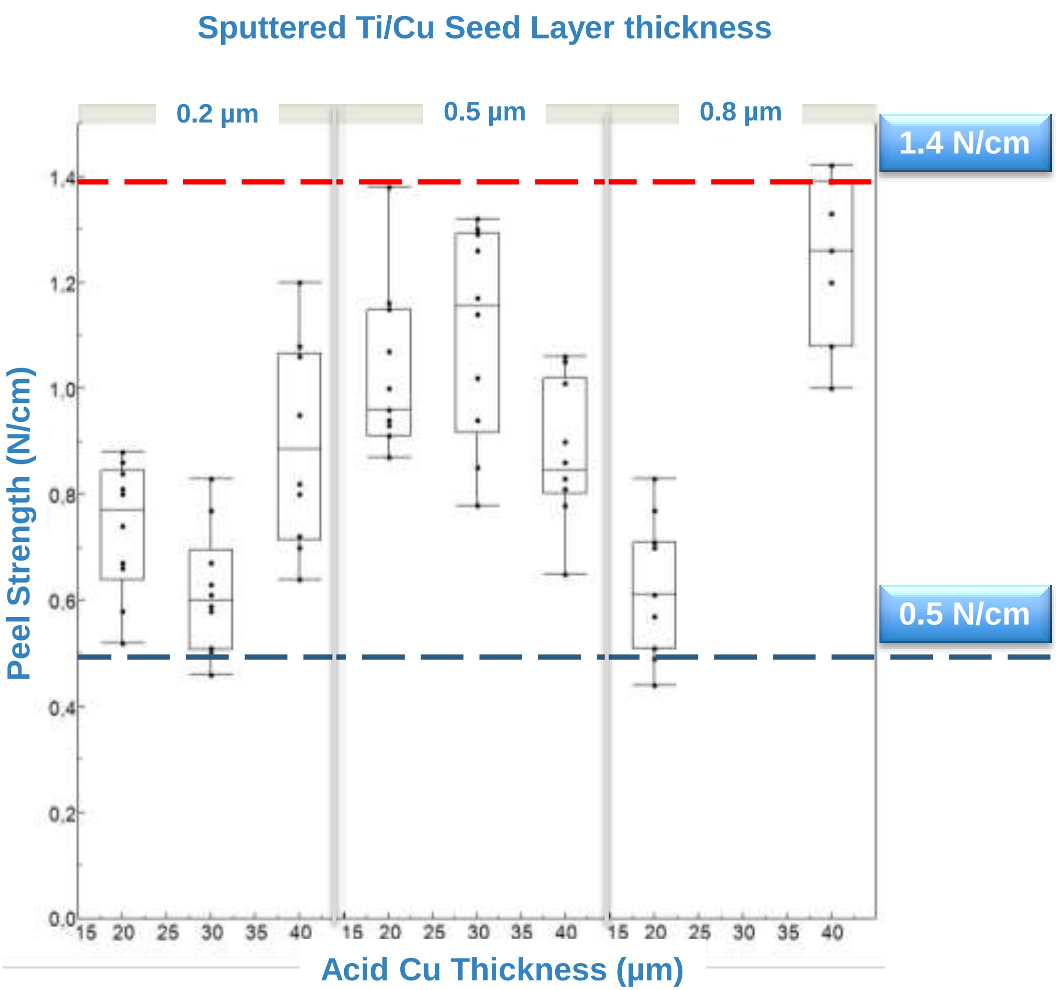
Adhesion Improvement by Additive Roughening Processes

Sputtered Seed Layer

Plating on Glass

Sputtering - Peel Strength on Glass

Integration into Interposer Manufacturing Process – Benchmark Peel Strength



Limitations of Sputtered Seed Layers for Adhesion on Glass

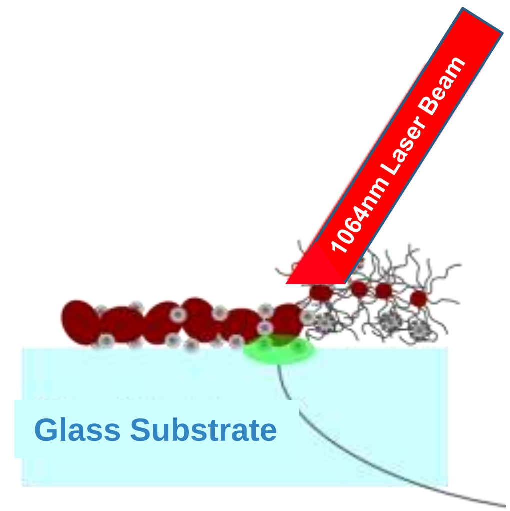
- Low adhesion regardless of seed layer thickness (0.4 – 1.4 N/cm)
- Tendency to delaminate for thick copper layers
- Difficult to sputter in high aspect ratio through holes for glass substrates

Sol Gel Exhibits Higher Peel Strength Than Sputtered Layers

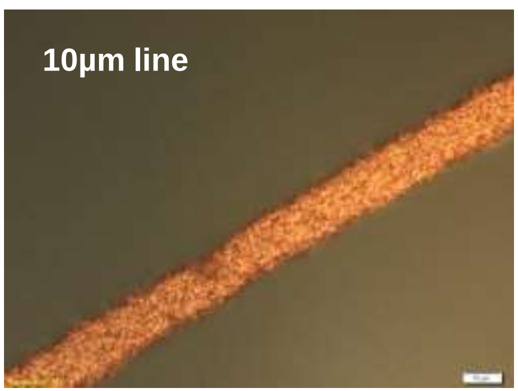
Nano Particle Inks

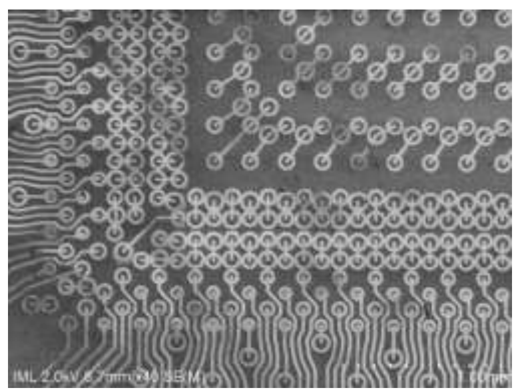
Plating on Glass
Adhesion Promoters for Glass

- Cleaning of the glass is crucial to obtain OH- rich surface
- Material is sprayed onto the glass
- Laser fixing creates covalent bonding with the glass
- Direct laser write or full glass coverage possible
- Wash off surplus if required
- Electroless copper is auto catalytically deposited



Early Prototype Structures

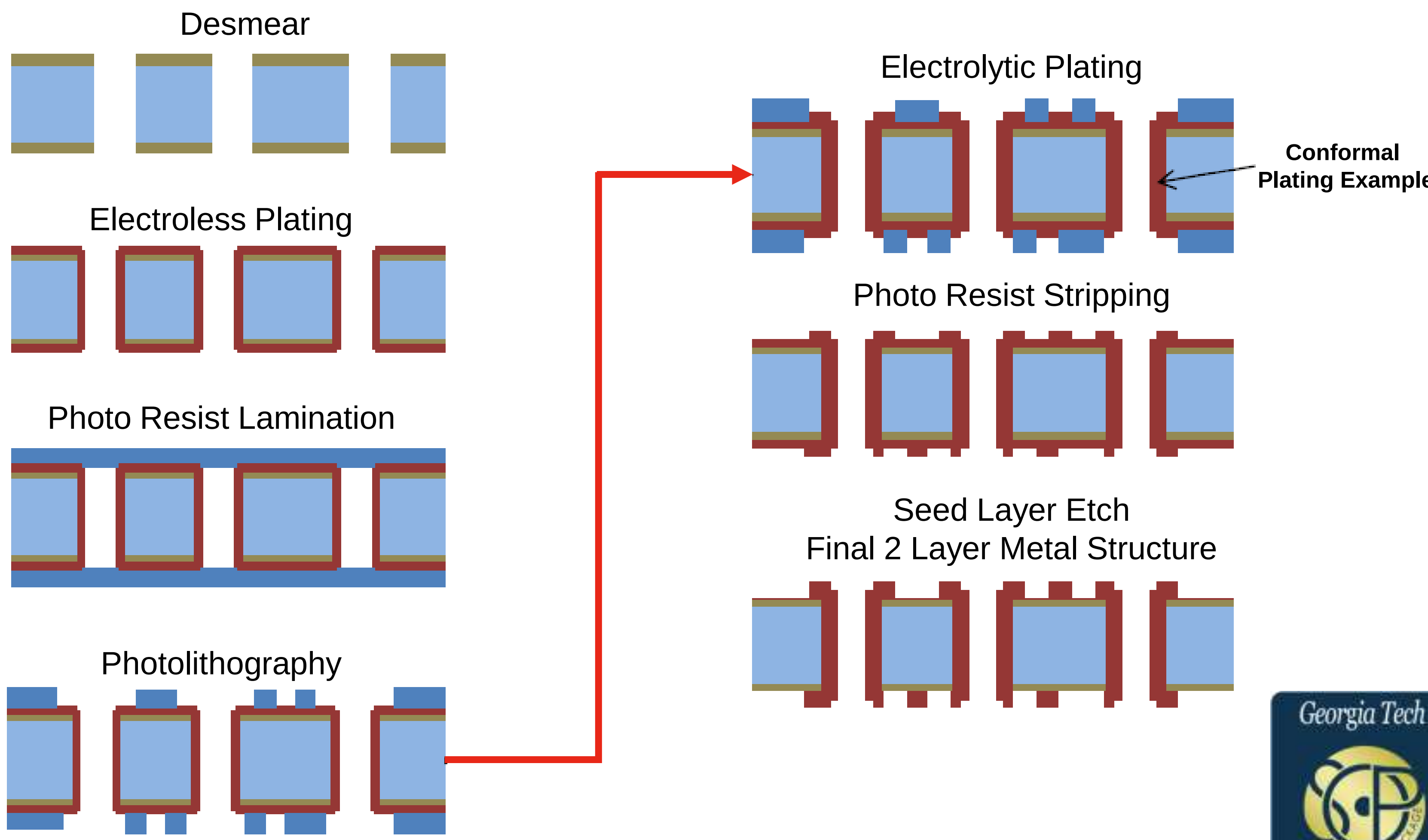




Adhesion Sufficient to Cause Cohesive Failure Mechanism in the Glass!

Polymer Laminated Glass

Plating on Glass
Polymer Laminated Glass

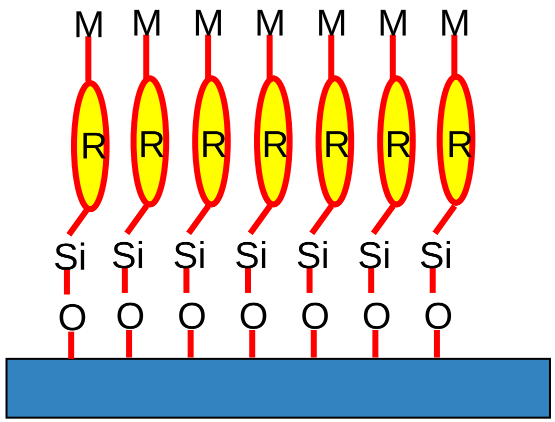


Process Sequence for a Two Layer Metal Structure

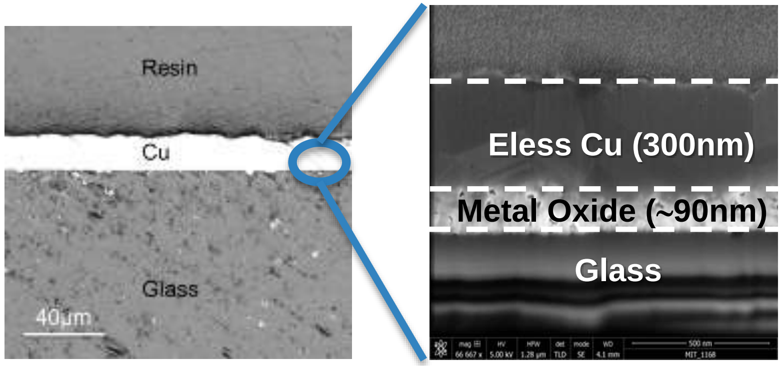
Metal Oxide Adhesion Promoter

Plating on Glass
Introduction

- Targets
  - Replace sputtering by wet chemical process for Glass, Si/SiO2 and Ceramic plating
  - Target > 5N/cm adhesion
- Approaches
  - Sol-Gel coating with metal oxide intermediate layer
  - Covalent bonds with Self Assembled Monolayer (SAM)
  - PhD project at CWRU

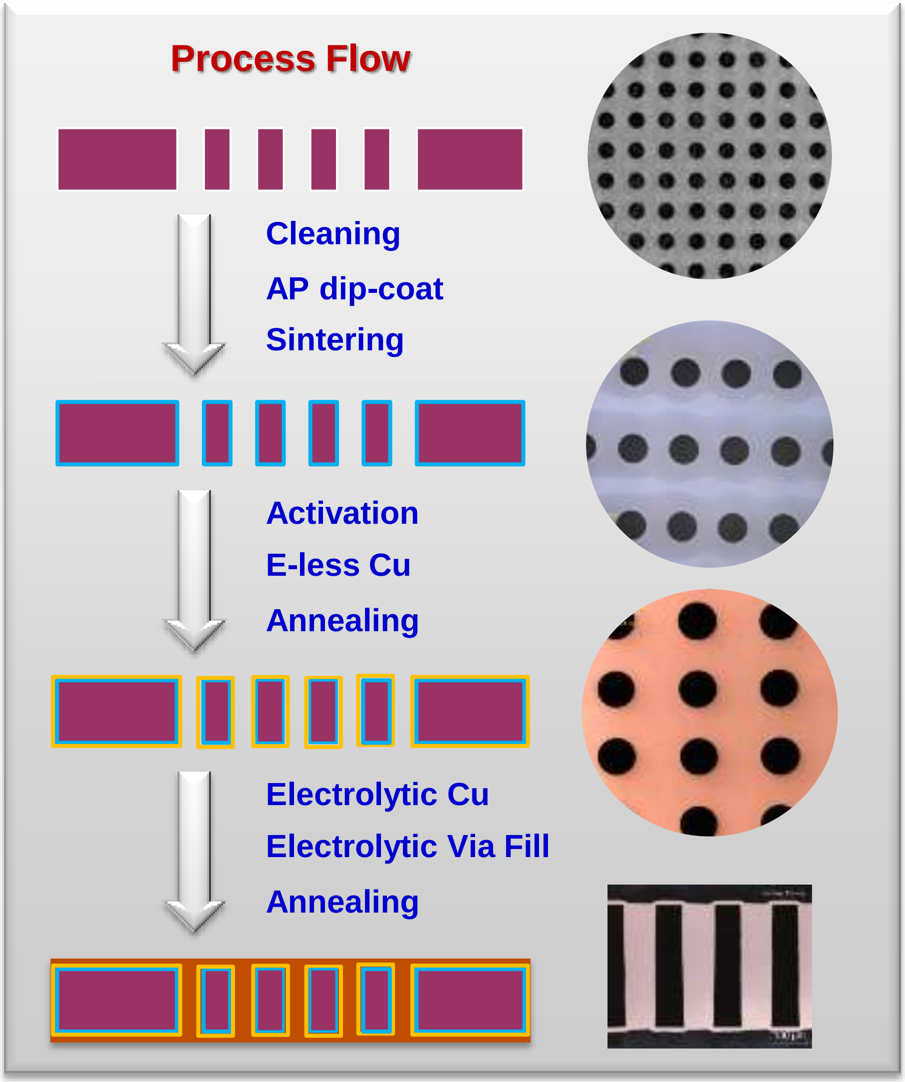


SAM



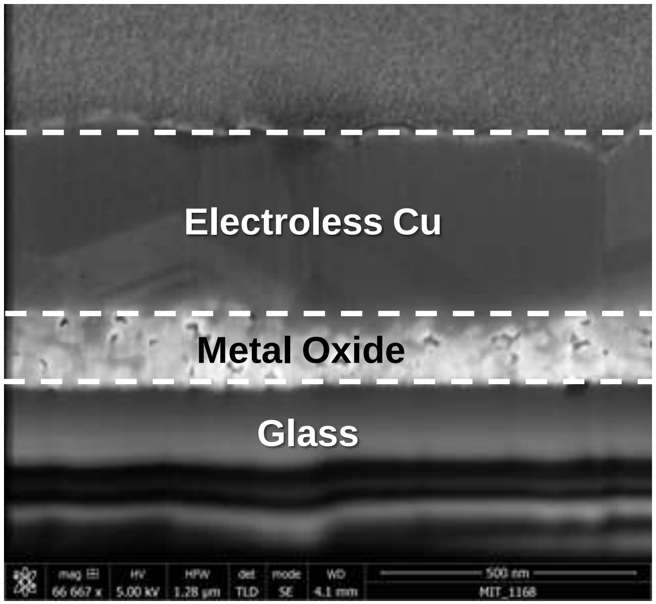
Plating on Glass
Process Flow for Plating on Glass with VitriCoat

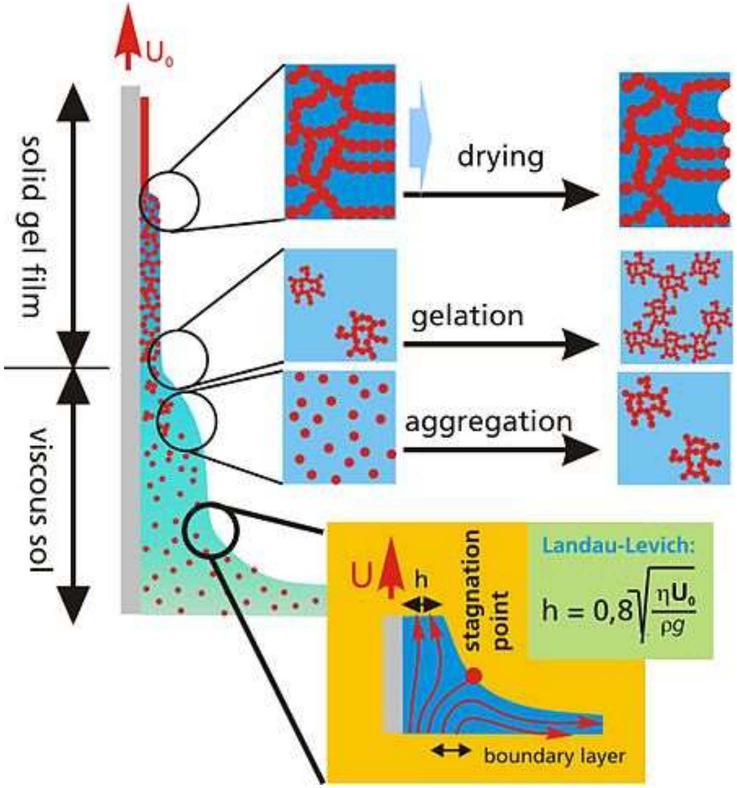
- Glass Cleaning
- Apply Adhesion Promoter
  – Metal Oxide Based
- Sintering
- Electroless Copper
- Electrolytic Cu Reinforcement
- X-Bridging
- Via Filling



Plating on Glass
Adhesion Promoter Thickness Control

Metal Oxide Intermediate Layer - Sol Gel Process – FIB Cross Section





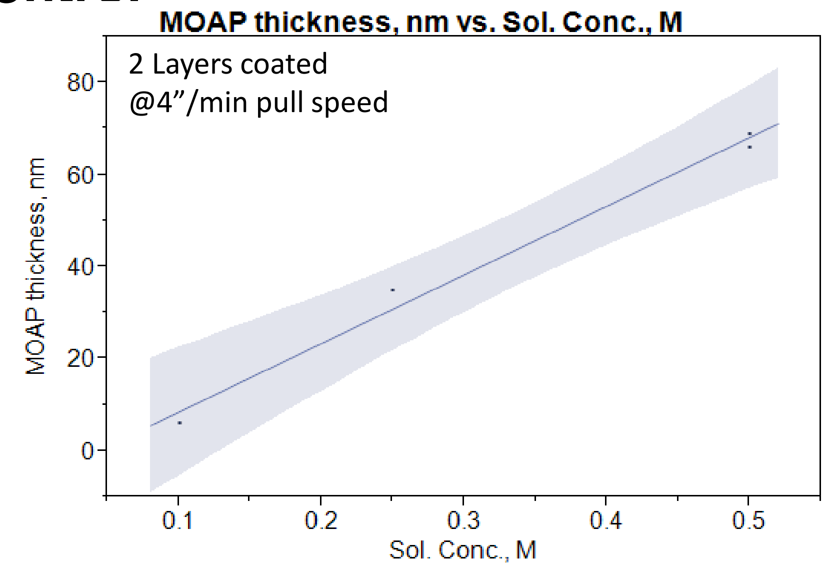
Principle of Sol Gel Process (Dip Coating)

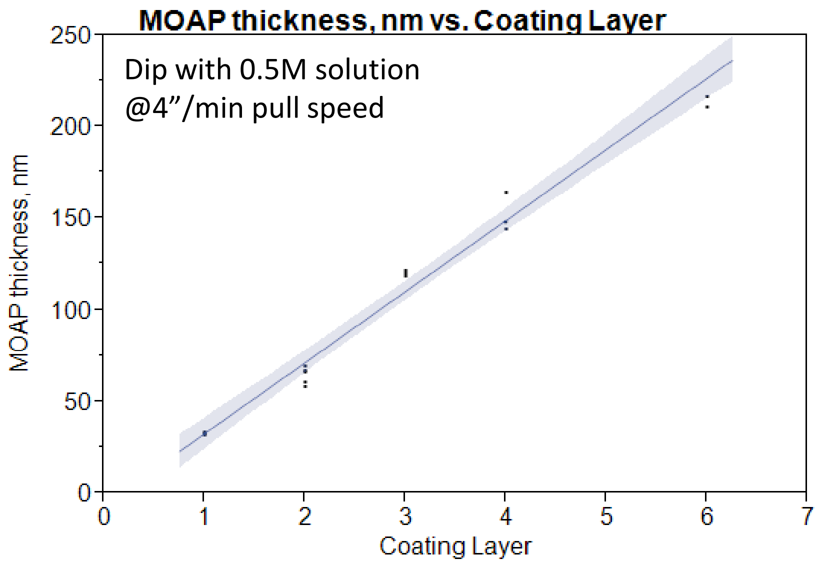
- The thickness of the metal oxide layer is tunable
- Nano scale mechanical anchoring and chemical bonding

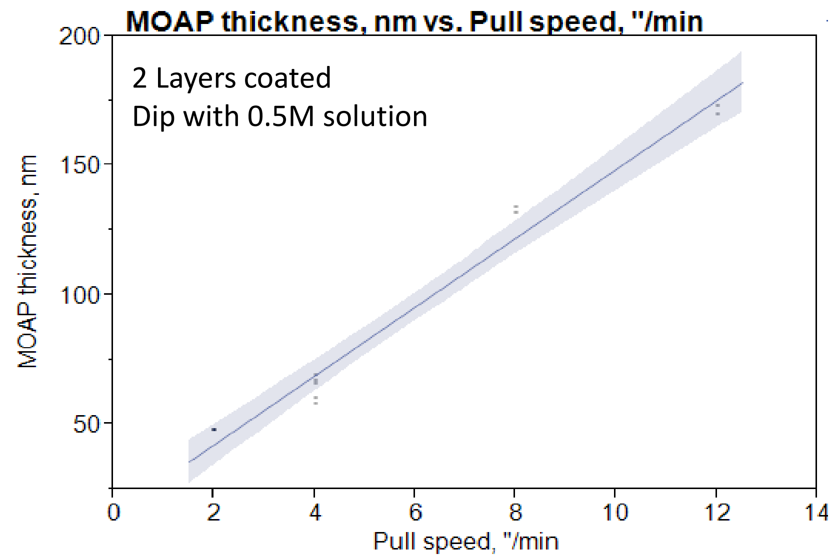
Adhesion Improvement by Additive Roughening Processes

Plating on Glass
Adhesion Promoter Thickness Control

- The thickness of the metal oxide layer can be controlled by
  - Concentration of solution
  - Pull speed
  - Number of coating layers







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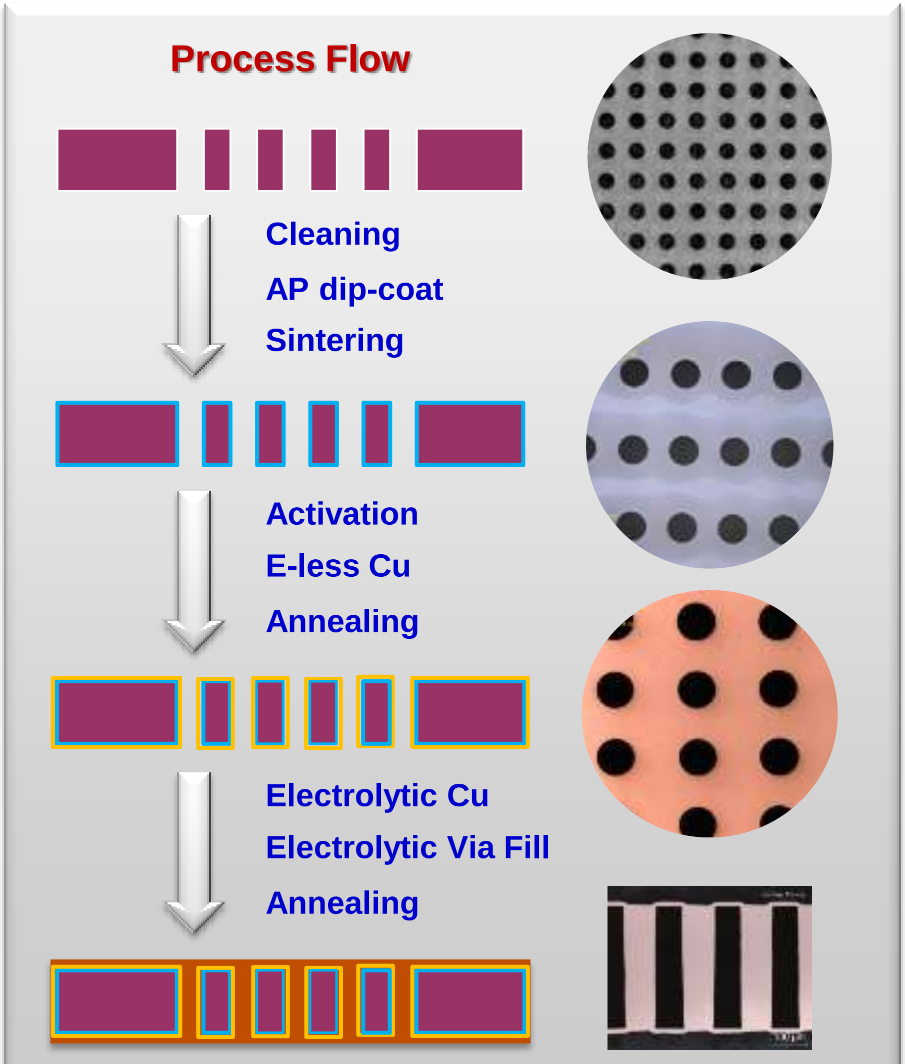
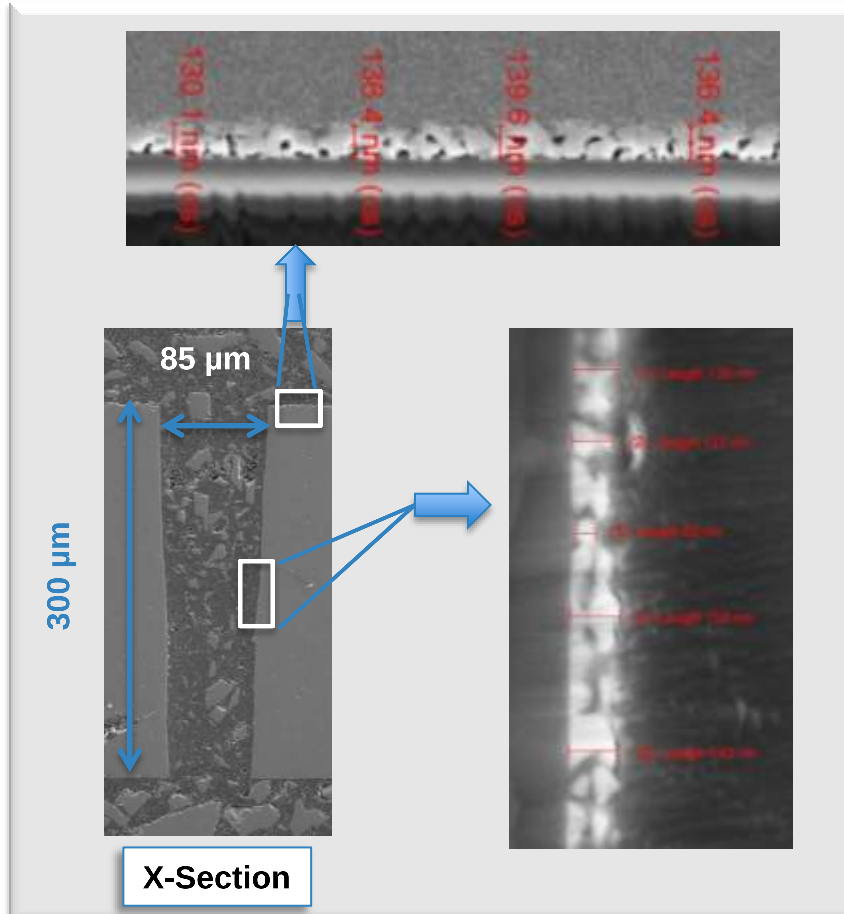
Plating on Glass

Electroless Copper and Electrolytic Copper Plating



- AP coating on the surface and inside the via hole

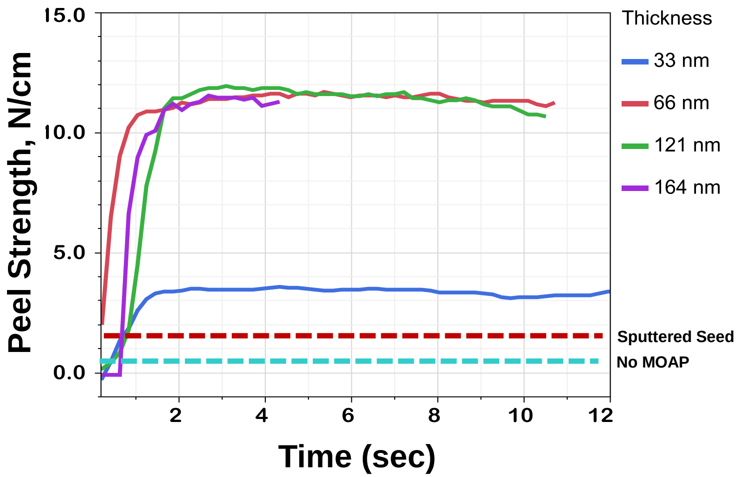


Plating on Glass
Peel Strength Versus Adhesion Promoter Thickness

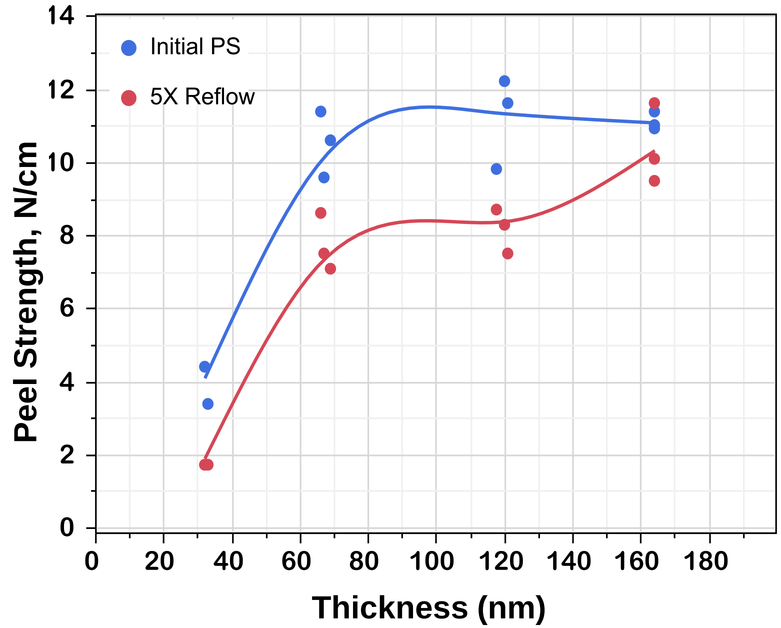
Asahi Glass

15µm Cu thickness

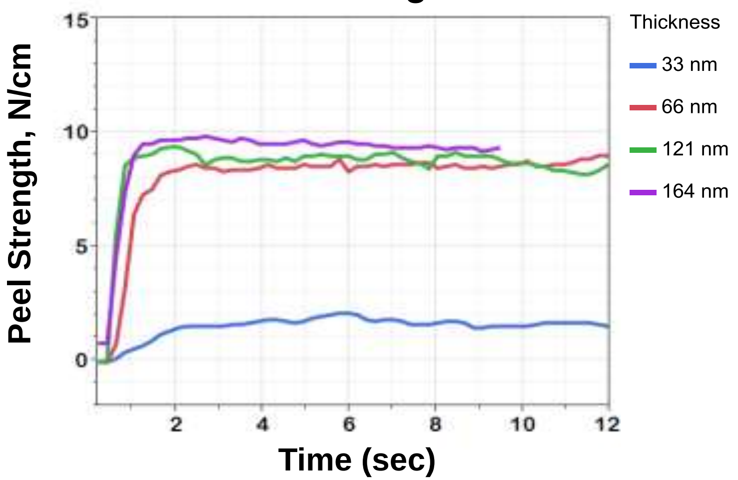
Initial Peeling Profile



Peel Strength vs. AP Thickness



5X RF Peeling Profile



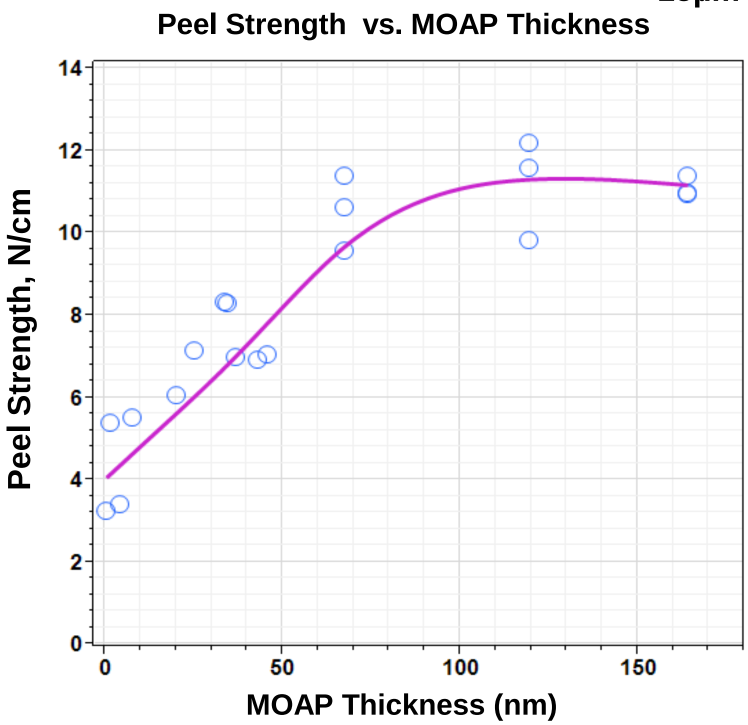
5 µm Cu w/o AP

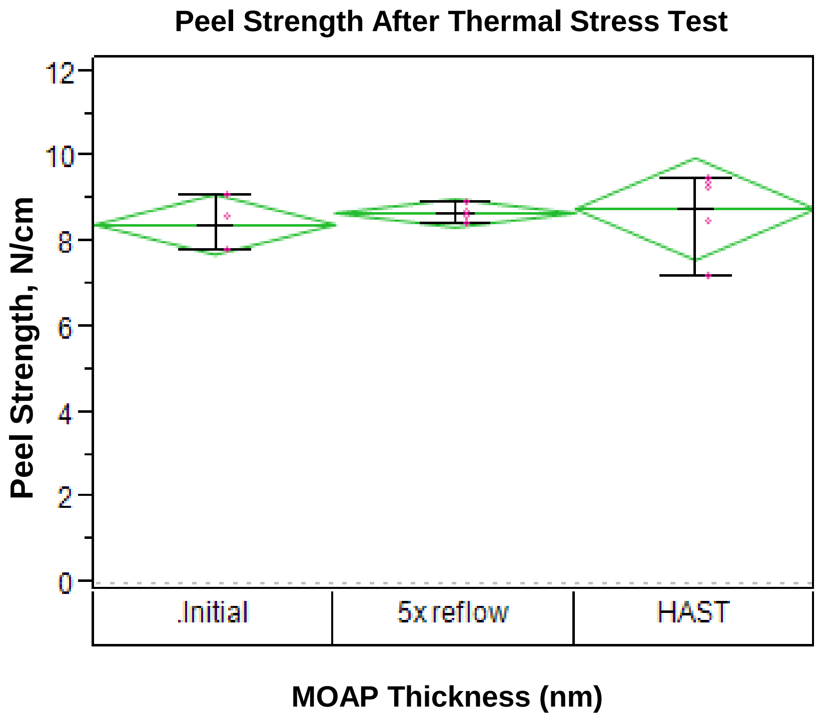
15 µm Cu w/ AP

Plating on Glass
Peel Strength Versus Adhesion Promoter Thickness

Corning Glass

15µm Cu thickness

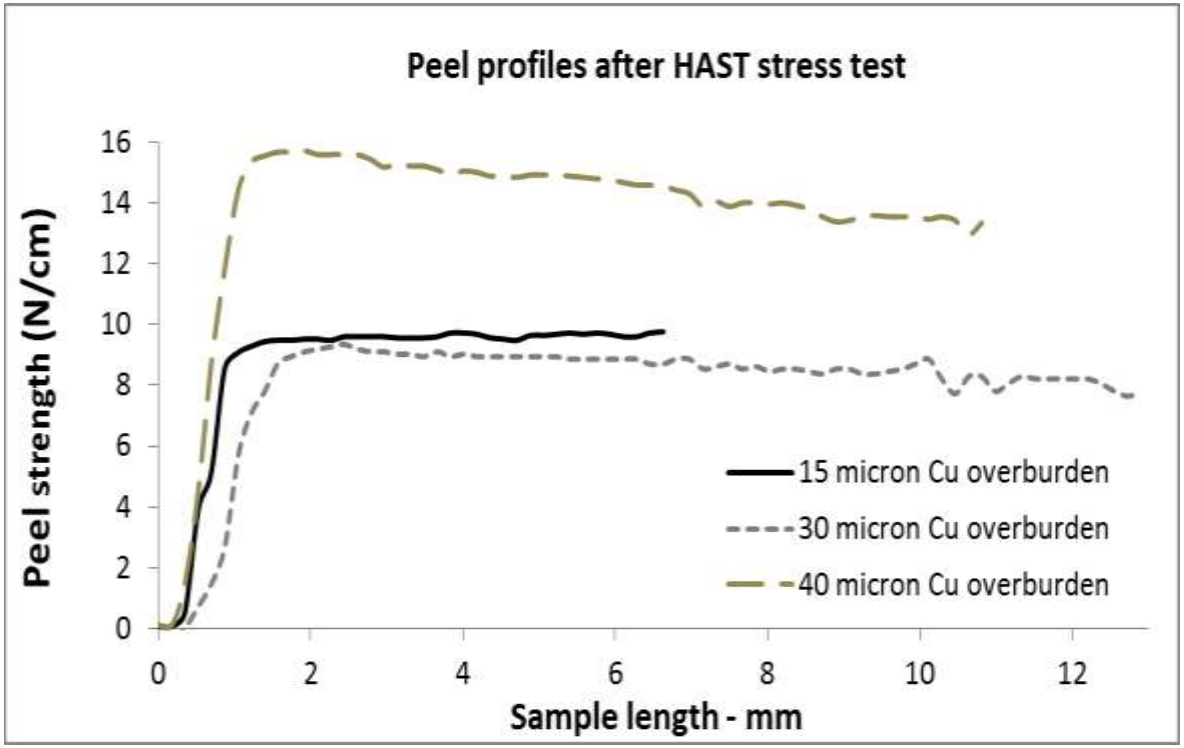




- Clear dependence of peel strength on AP thickness
- Peel strength of 5-6 N/cm achieved with ~ 10nm AP thickness
  - Fine line patterning benefits
- No significant impact of thermal excursion on performance

Plating on Glass
Peel Strength vs. Copper Thickness

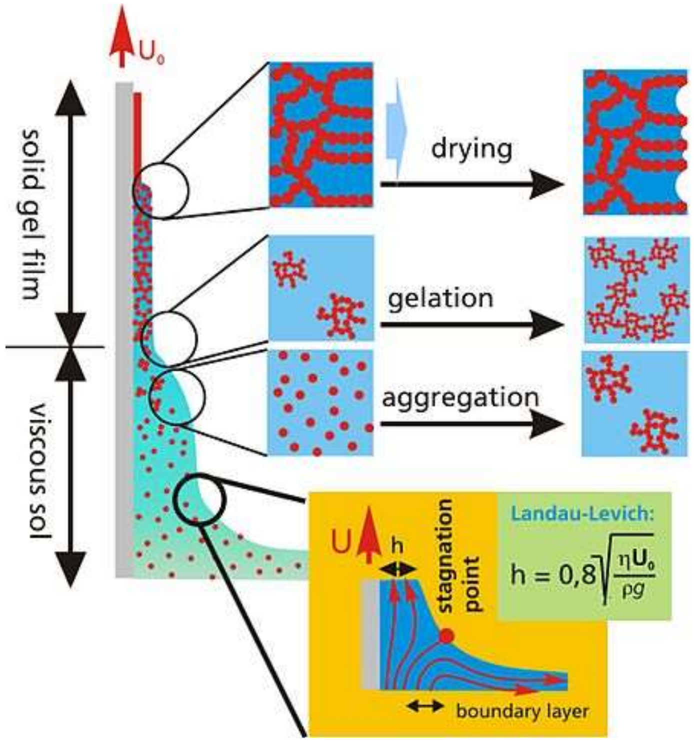
Corning Glass



- Peel strength increase as we normalise to ~35µm copper thickness
- No degradation of peel strength up to 40µm overburden
- No adhesion issues when CMP required

Plating on Glass
Conclusions – Adhesion Promoter

- The use of VitroCoat provides excellent adhesion to ultra smooth glass
- Ultra thin AP (~10nm) also provide good adhesion (6N/cm)
- Independent of glass type and roughness
- Adhesion is sufficient to withstand
  – Stresses created by electroless copper
  – Stresses created by electrolytic copper
  – Thermal stresses, both reflow and HAST
  – CMP processing
- Without issues with through holes
  – Tested down to 20µm diameter 10:1 AR
- Without issues with blind micro vias
  – Blind vias down to 35um diameter 2:1 AR



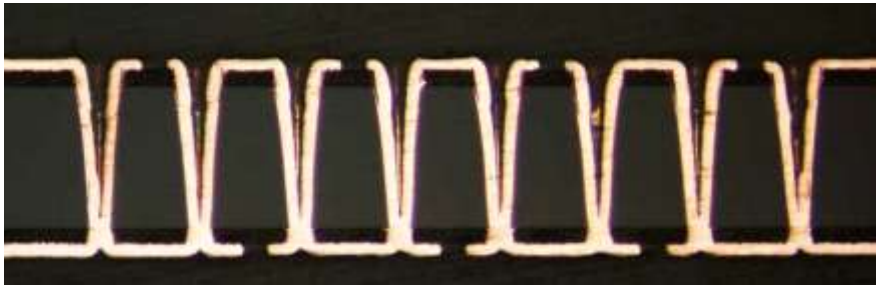
Principle of Sol Gel Process (Dip Coating)

Plating on Glass

Electroless Copper and Electrolytic Copper Plating

Process is Plating Tool and Electrolyte Dependant

- Hole Shape
  - V shaped holes will always fill "bottom
    up" like a blind micro via
  - Pulse parameters will have to be optimized for these hole shapes
  - Iron mediated electrolytes will offer best chance for success



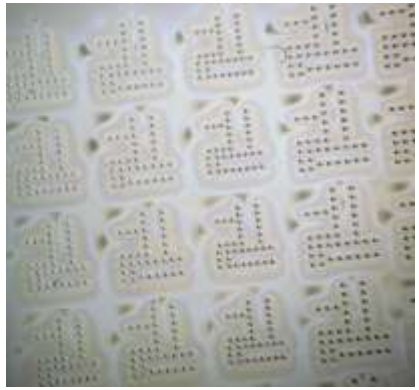
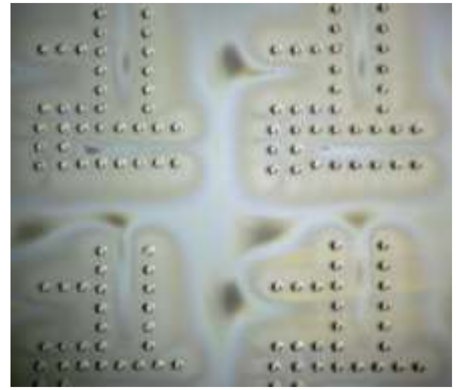
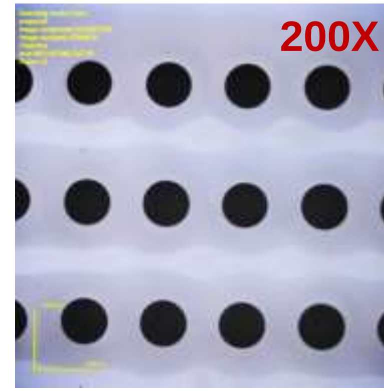
Produced in Vertical Plating Systems at Georgia Tech

- No Industry Capability Yet Established
  - Plating tools in IC Substrate manufacturing
  - Conformal plating, and through hole filling
  - Untested as yet on thin glass

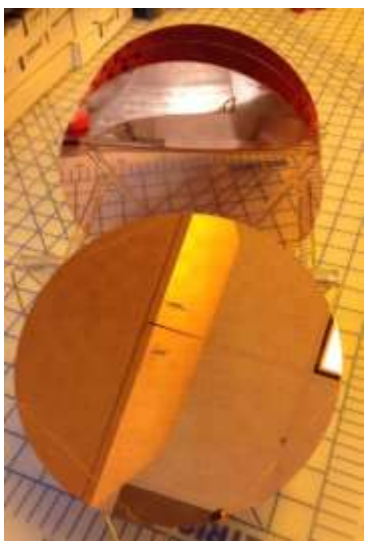
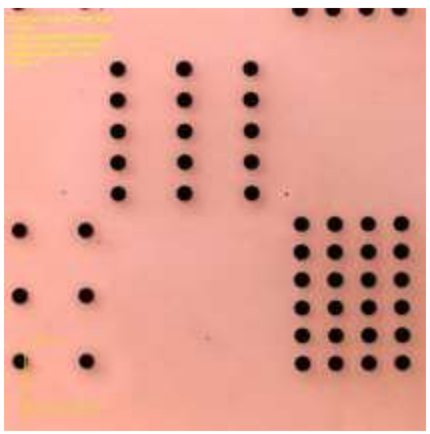
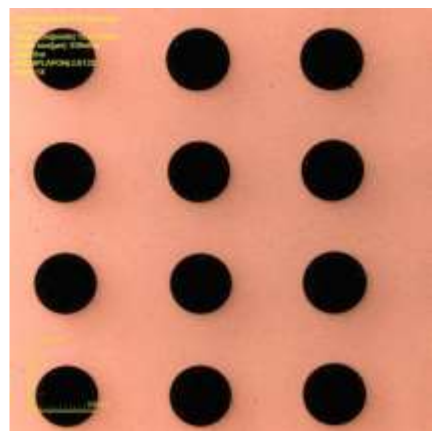
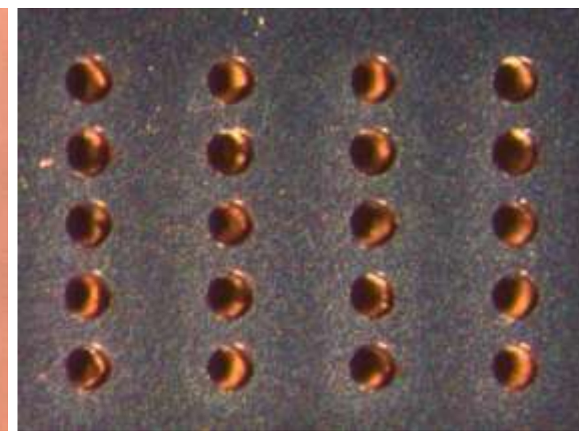
60-25 Hole Ø Top/Bottom - 100µm Glass
15µm ZIF Polymer - 22µm Cu Overburden

Atotech - Your Systems Technology Partner!

Plating on Glass
Electroless Copper and Electrolytic Copper Plating

Glass Coated with Adhesion Promoter and Sintered

Electroless Copper and Annealing **Post Electrolytic Cu**

No Through Hole Blockages – No Blistering or Adhesion Loss!

Plating on Glass
Electroless Copper and Electrolytic Copper Plating

- Double sided plating using reverse pulse plating with insoluble anodes and an iron redox system
- Void free filling with low surface overburden required
- Challenges
  - Thin and fragile substrates
  - Non-Cylindrical tapered vias with aspect ratios > 3:1 AR

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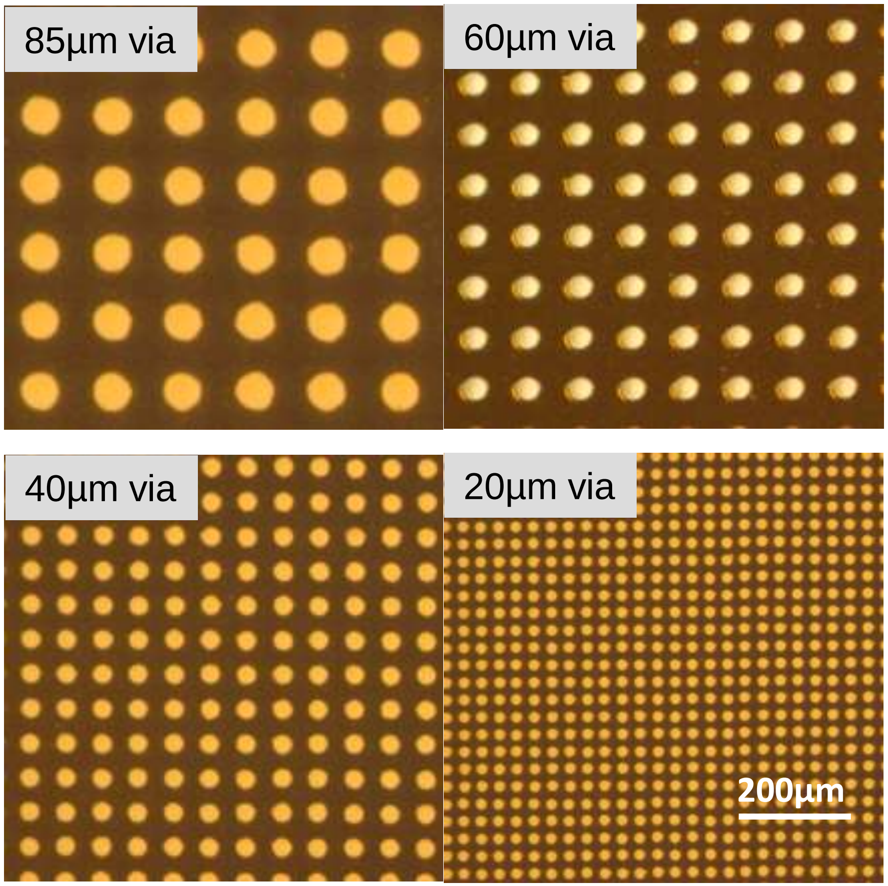
Plating on Glass
Electroless Copper and Electrolytic Copper Plating

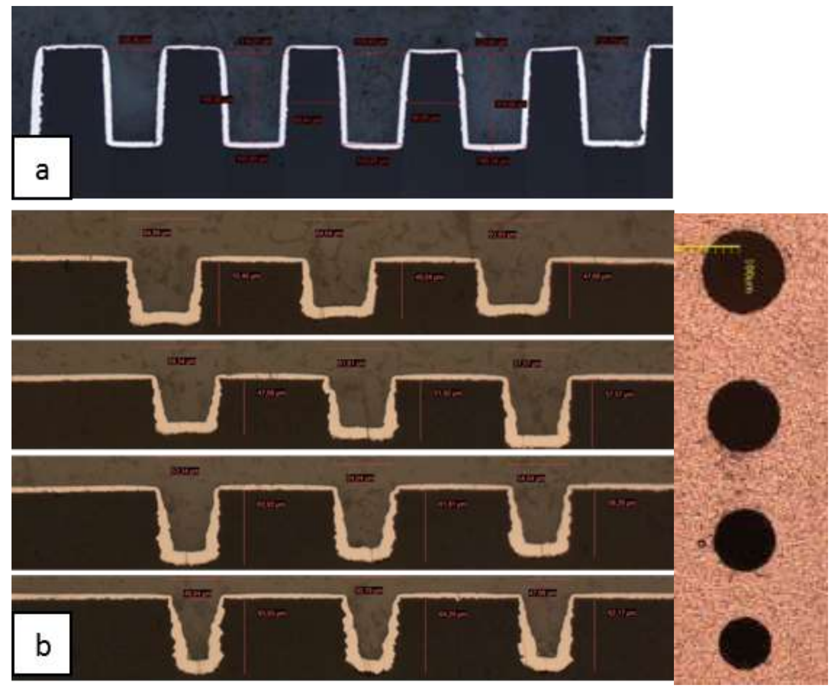
Through Glass Via (TGV's) Plating

Top view of TGVs (200 or 300µm Glass)



Blind Micro Via (BMV's) Plating

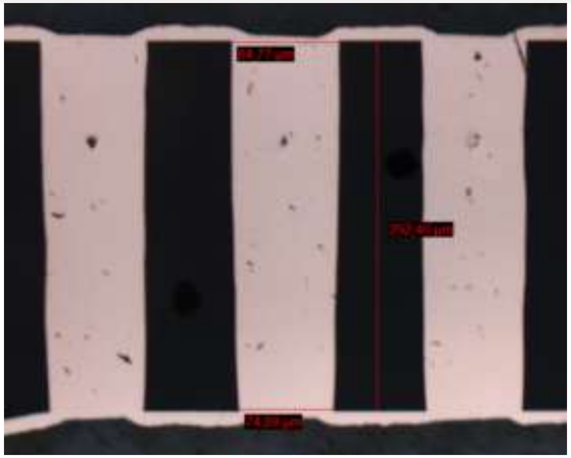
(a) Ø120µmx170µm,
(b) Ø65 ~35µmx 60µm.



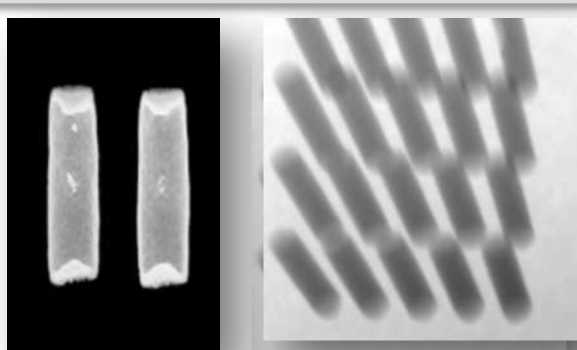
No Through Hole Blockages – No Blistering or Adhesion Loss!

Plating on Glass
Through Hole Filling and Blind Via Filling Status

TGV's

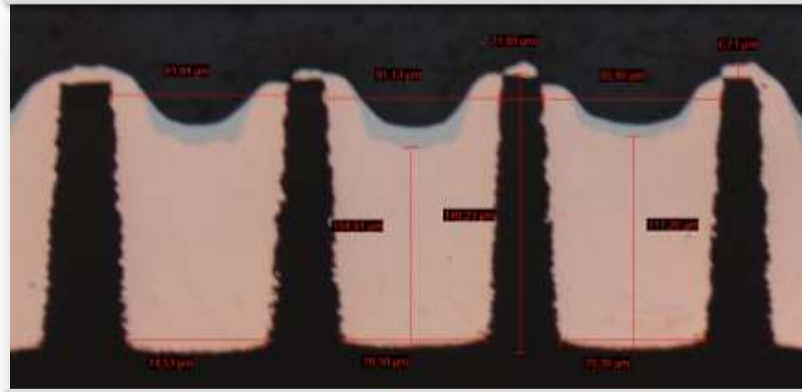


300µm by ~ Ø 80 µm TGV 3.6: 1 AR

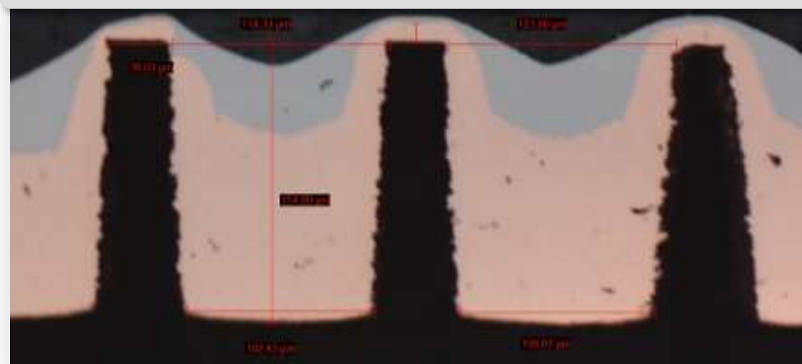


BMV's

170 by Ø 90µm BMV



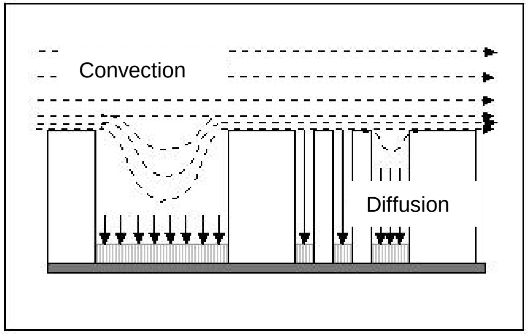
170 by Ø 120µm BMV

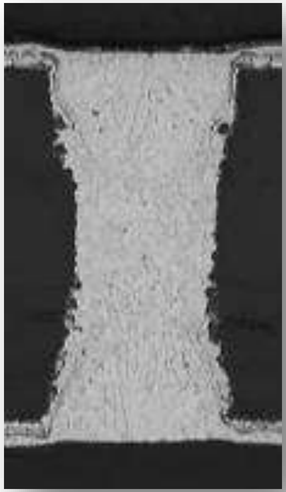


- Copper overburden ~ 10µm, some optimisation still required

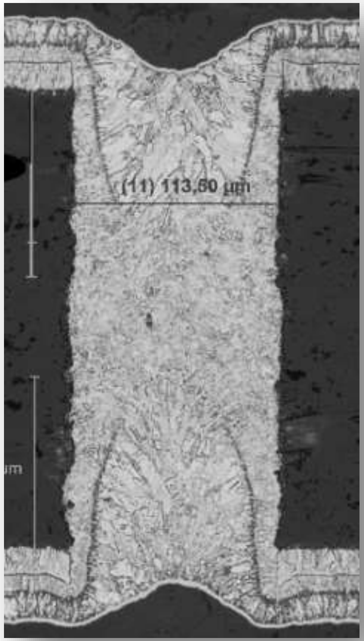
Plating on Glass
Multiplate Through Hole Filling Scaling

- Feasibility studies for Scaling of THF Approach

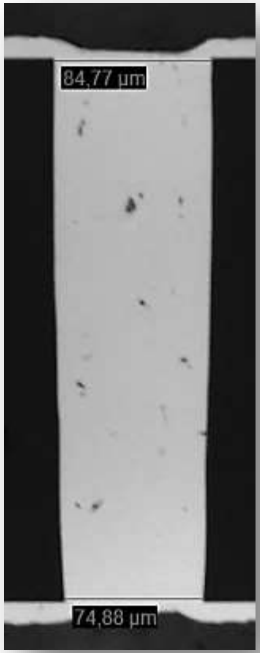




200 x 100 µm
Panel Plating



275 x 115 µm
Std. BTT-SC



300 x 80 µm
PoG (3.6 : 1 AR)

295 x 45 µm
CNSE (6.5 : 1 AR)

New X-Bridging Approach

Electrical Characterisation
Fine Line Patterning

Plating on Glass

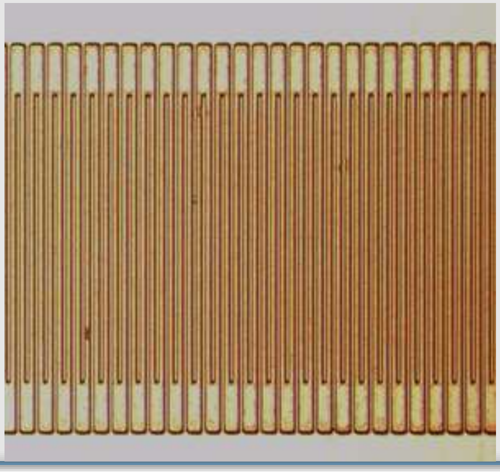
Initial Fine Line Patterning Results SAP on Glass

Source: Georgia Tech

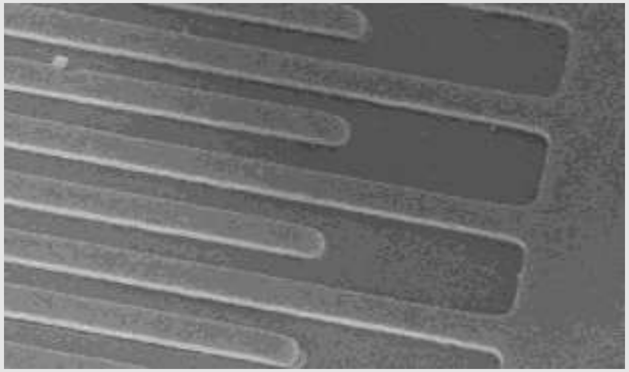
Process Flow

- Substrate cleaning
- VitroCoat AP coating
- Electroless Cu plating
- Annealing
- Novalink®
- Photolithography
- Electrolytic Cu plating
- Photoresist stripping
- Annealing
- CupraEtch™ DE

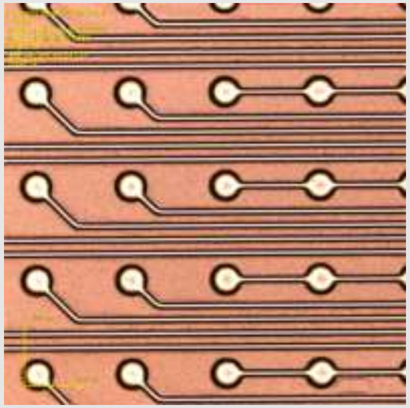
L/S: 6/6µm, Before Cu seed layer etching



L/S=9/9 µm,
After Cu seed layer etching



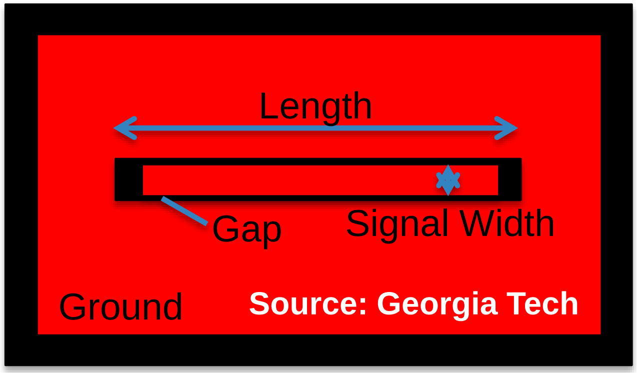
150µm Pitch / 50µm Pad
L/S: 11/11µm,
Before Cu seed layer etching

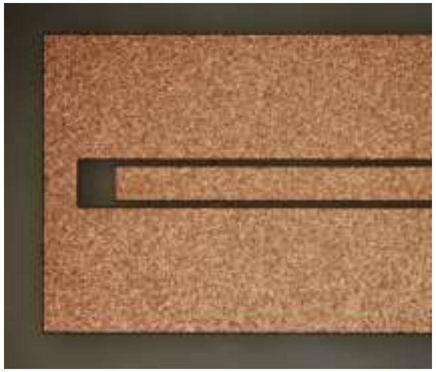


Plating on Glass

Coplanar Waveguide (CPW) Design and Sample Fabrication

- CPW Design
  - Length
    - 16200, 112000, 6200µm
  - Gap
    - 26.5, 19.0µm
  - Signal Width
    - 170, 120µm
- Glass Type
  - Corning
    - Low CTE glass
- Georgia Tech
  - Fabricated, tested
  - Within consortium
    - Further tests ongoing
- IZM Cooperation
  - Demonstrators
  - Characterisation





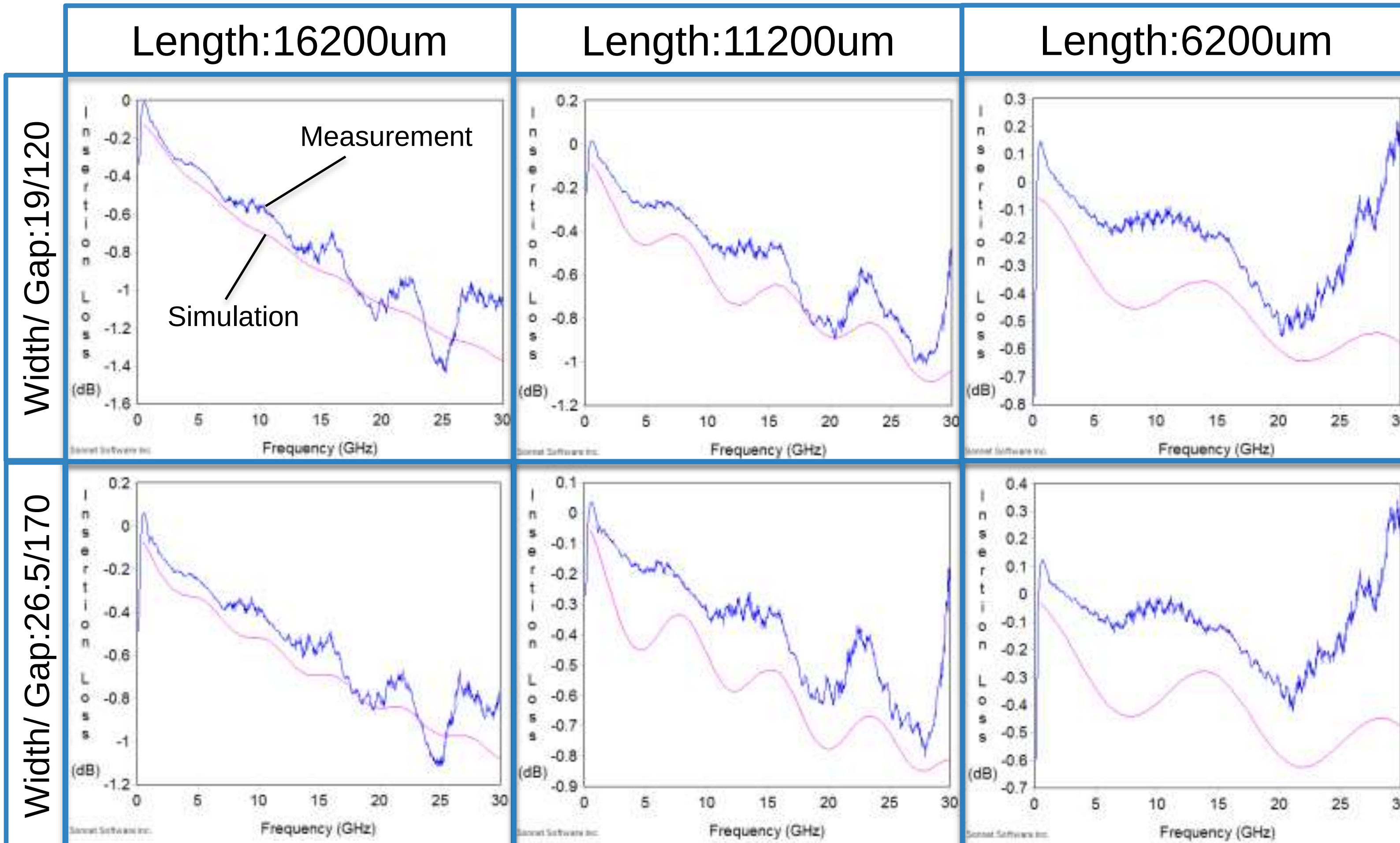
Length / µm	Designed		Fabricated		Measurement
	Gap / µm	Width / µm	Gap / µm	Width / µm	
16200	26.50	170.00	28.80	167.20	Measurable
16200	19.00	120.00	20.28	117.35	Measurable
11200	26.50	170.00	28.00	168.23	Measurable
11200	19.00	120.00	18.65	120.45	Measurable
6200	26.50	170.00	24.88	169.05	Measurable
6200	19.00	120.00	17.85	118.48	Measurable

ATOTECH

Plating on Glass

S-Parameters Simulation and Measurement

Source: Georgia Tech



- Good correlation between simulation and measured results
- AP layer has no effect on electrical performance of transmission lines

ATOTECH

Plating on Glass
Summary

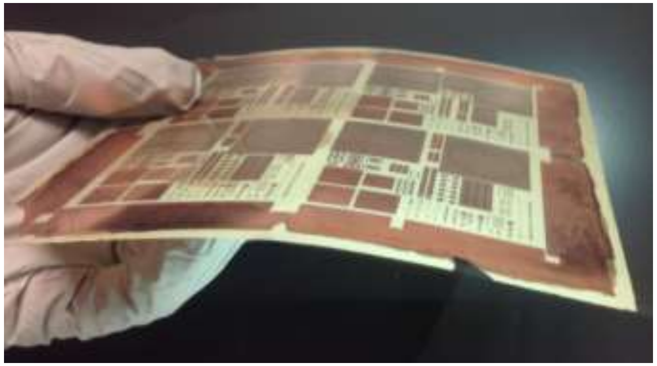
- Processes for Glass Interposer Manufacturing are Evolving
  - Adhesion promoter for bare glass developed
  - On bare glass electroless / electrolytic Cu adhesion is the major challenge

Atotech's Multiplate System

- Polymer laminated glass has a POR from Atotech

(Source: Georgia Tech)

- Equipment for Glass Interposer Manufacturing
  - Challenge is to handle wet chemical processing of thin glass materials



- Atotech production solutions, horizontal and vertical need to be qualified with thin glass
- Plating parameters / limits must be established

30µm Thick Polymer Laminated Glass

- TCoO, manufacturability and assembly yield will drive market introduction

Supporting The Next Generation of Packaging Substrates

Thank you for your attention!